

# 君正® Halley5 核心板

数据手册

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北京君正集成电路股份有限公司  
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# 君正® Halley5

## 数据手册

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# 1 概述

## 1.1 简介

Halley5 核心板是一款基于 X2000 设计的物联网设备设计的双核高性能、低成本的无线局域网模块, 最高 1.2GHz 主频、内部集成 1Gb LPDDR3, 750MHz。核心板还包括一个 2Gb SPI NAND Flash, Wi-Fi IEEE 802.11 b/g/n/ac 双频、Bluetooth 5.0 和 Bluetooth Low Energy 二合一模块。它也为各种外设接口提供了一个引脚数为 144 的邮票孔接口, 可以外扩液晶显示、音频、相机、以太网、SD 卡、USB OTG、SPI、I2C、UART、PWM、NEMC、ADC 等。可广泛应用, 如无线对讲、智能玩具、智能网关、智能家居等。

Halley5 核心板可以运行最新的 Linux 内核和 TCP / IP 堆栈。搭载高性能 XBurst CPU, 支持硬件浮点单元 (FPU), SIMD 加速指令, 支持各类语音识别、图像识别、降噪、消回音、APE/FLAC 解码等算法。

## 1.2 Halley5 结构



### 1.3 Halley5 功能参数

- 尺寸规格: 38mm x52mm X 1mm
- CPU 工作频率: 最高 1.2GHz
- 内存: 1G bits LPDDR3 (嵌入 X2000)
- 外部存储: 2G bits SPI NAND Flash (兼容 SPI NOR Flash)
- Wi-Fi: 双频 Wi-Fi 802.11 b/g/n/ac
- Bluetooth: Bluetooth 5.0 with BLE, 2.1 EDR
- 工作电压: DC 5V
- Wi-Fi and Bluetooth 参数
  - ☆IEEE 802.11 b/g/n/ac dual-band radio
  - ☆Bluetooth 5.0 with integrated class 1.5 PA
  - ☆ Concurrent Bluetooth and WLAN operation, simultaneous BT/WLAN reception with a single antenna
  - ☆WLAN host interface options: - SDIO v3.0 and backward compatible with SDIO v2.0 host interfaces. — up to 208 MHz clock rate in SDR104 mode
  - ☆BT host digital interface: -UART (up to 4 Mbps)
  - ☆Bluetooth Low Energy support
- 物理接口
  - ☆Display: 8/9/16 bits SLCD & 24 bits RGB LCD & 2 lane MIPI
  - ☆PWM x16 & TCU x8
  - ☆I2C x5
  - ☆MSC x1
  - ☆NEMC 8/16bit
  - ☆SPI x2
  - ☆Smart card x1
  - ☆UART x9
  - ☆I2S x3
  - ☆Analog MIC x1
  - ☆Digital MIC x4
  - ☆ADC x6
  - ☆Headphone x1
  - ☆SPDIF IN & SPDIF OUT
  - ☆USB 2.0 OTG
  - ☆Ethernet MAC: (RGMII)x1
  - ☆Camera: (8/10 bit DVP & 8/10/12 bit raw VIC)& (2x2 lane MIPI& 4 lane MIPI)

温度:

- 工作温度: -40~85℃

## 2 外部接口

### 2.1 外部管脚

Halley5 核心板被设计成邮票孔接口。1 脚左上角逆时针方向放置,孔距为 1.2mm。

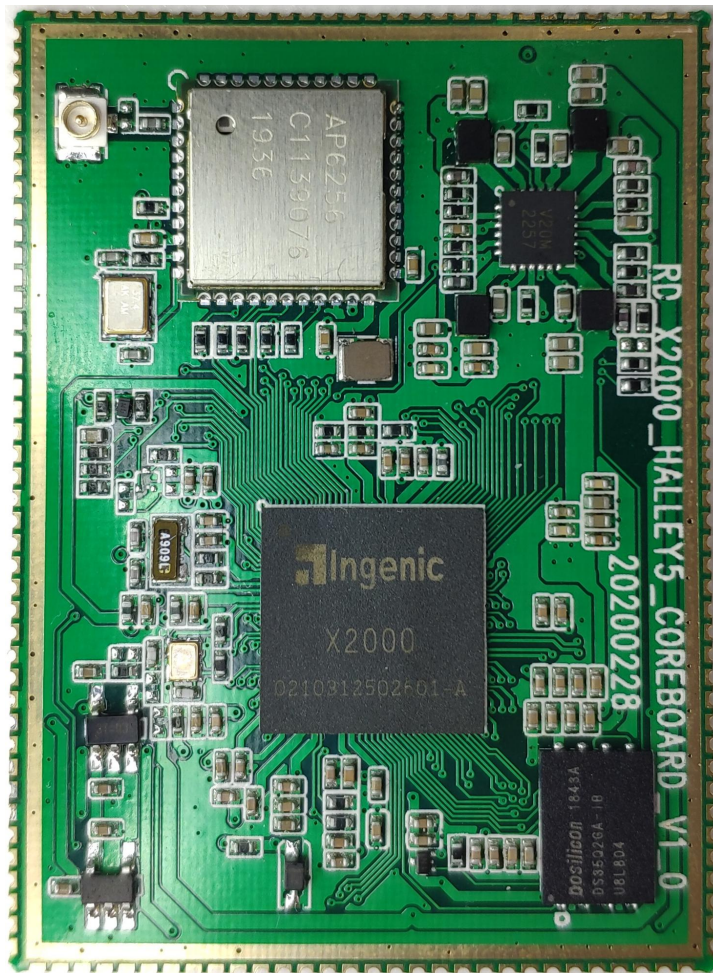


图 2-1 PCBA 顶部视图

引脚编号	引脚名称	引脚描述	类型
1	LCD_D20/RGMAC1_MDIO	SD4: NEMC DATA4	IO
		LCD_D20: LCD DATA20	0
		RGMAC1_MDIO: RGMII1 management data	IO
		PB20: GPIO group B bit 20	IO
2	LCD_D19/RGMAC1_MDC	SD3: NEMC DATA3	IO
		LCD_D19: LCD DATA19	0
		RGMAC1_MDC: RGMII1 management clock	0
		PB19: GPIO group B bit 19	IO
3	GND	GND	P
4	GND	GND	P
5	VSYS	VSYS	PI
6	VSYS	VSYS	PI
7	GND	GND	P
8	1V8P	1V8P	PO
9	GND	GND	P
10	3V3P	3V3P	PO
11	LCD_PCLK/SLCD_CE_N	SD8: NEMC DATA8	IO
		LCD_PCLK: LCD pixel clock	0
		SLCD_CE_N: Smart LCD chip select signal	0
		PB24: GPIO group B bit 24	IO
12	LCD_VSYNC/SLCD_DC	SD9: NEMC DATA9	IO
		LCD_VSYNC: LCD frame sync	0
		SLCD_DC: Smart LCD data/command select signal	0
		PB25: GPIO group B bit 25	IO
13	LCD_HSYNC/SLCD_WR	SD10: NEMC DATA10	IO
		LCD_HSYNC: LCD line sync	0
		SLCD_WR: Smart LCD write signal	0
		PB26: GPIO group B bit 26	IO
14	LCD_DE/SLCD_TE	SD11: NEMC DATA11	IO
		LCD_DE: LCD data enable	0
		SLCD_TE: Smart LCD tearing effect signal	I
		PB27: GPIO group B bit 27	IO
15	SSI0_CLK	SD15: NEMC DATA15	IO
		SSI0_CLK: SSI0 clock output	0
		UART9_TXD: UART9 transmitting data	0
		PB31: GPIO group B bit 31	IO



16	SSIO_CEO	SD12: NEMC DATA12 SSIO_CEO_N: SSI0 chip enable0 UART8_RXD: : UART8 receiving data PB28: GPIO group B bit 28	IO 0 I IO
17	SSIO_DR	SD13: NEMC DATA13 SSIO_DR: SSI0 data input UART8_TXD: UART8 transmitting data PB29: GPIO group B bit 29	IO I 0 IO
18	SSIO_DT	SD14: NEMC DATA14 SSIO_DT: SSI0 data output UART9_RXD: UART9 receiving data PB30: GPIO group B bit 30	IO 0 I IO
19	GPI033_PC28	PC28: GPIO group C bit 28	IO
20	UART3_TXD	UART3_TXD: UART3 transmitting data I2C4_SDA: I2C4 serial data PC26: GPIO group C bit 26	0 IO IO
21	UART3_RXD	UART3_RXD: UART3 receiving data I2C4_SCK: I2C4 serial clock PC25: GPIO group C bit 25	IO 0 IO
22	UART2_TXD	UART2_TXD: UART2 transmitting data I2C3_SDA: I2C3 serial data PWM1: PWM1 data output TCU0_IN1: TCU0 data input1 PD31: GPIO group D bit 31	0 IO 0 I IO
23	UART2_RXD	UART2_RXD: UART2 receiving data I2C3_SCK: I2C3 serial clock PWM0: PWM0 data output TCU0_IN0: TCU0 data input0 PD30: GPIO group D bit 31	I 0 0 I IO
24	GND	GND	P
25	CIM_VIC_MCLK	EXCLK: 24 MHz clock output CIM_VIC_MCLK: 24 MHz clock output PE24: GPIO group E bit 24	0 0 IO
26	GPI018_PD18	PD18: GPIO group D bit 18	IO
27	WKUP_N	WKUP_N: WAKE UP	I
28	DRVVBUS	DRV_VBUS: USB OTG VBUS driver control signal PE22: GPIO group E bit 22	0 IO
29	PPRST_N	PPRST_N: RTC power on reset and RESET-KEY reset input	I
30	GND	GND	P



31	I2C3_SDA	I2C3_SDA: I2C3 serial data I2S2_RX_BCLK: I2S2 input bit clock PA17: GPIO group A bit 17	I0 I I0
32	I2C3_SCK	I2C3_SCK: I2C3 serial clock I2S3_TX_BCLK: I2S3 output bit clock PA16: GPIO group A bit 16	0 0 I0
33	BOOT_SEL2	BOOT_SEL2: boot configuration PE27: GPIO group E bit 27	I I0
34	BOOT_SEL1	BOOT_SEL1: boot configuration PE26: GPIO group E bit 26	I I0
35	BOOT_SEL0	BOOT_SEL0: boot configuration PE25: GPIO group E bit 25	I I0
36	VIC_D10/I2S2_RX_DATA0	VIC_D10: VIC DATA10 I2S2_RX_DATA0: I2S2 data input bit 0 PA10: GPIO group A bit 10	I I I0
37	VIC_D11/I2S2_RX_DATA1	VIC_D11: VIC DATA11 I2S2_RX_DATA1: I2S2 data input bit 1 PA11: GPIO group A bit 11	I I I0
38	CIM_VIC_VSYNC/I2S2_RX_DATA3	CIM_VIC_VSYNC: CIM/VIC line sync I2S2_RX_DATA3: I2S2 data input bit 3 PA13: GPIO group A bit 12	I I I0
39	CIM_VIC_PCLK	CIM_VIC_PCLK: CIM/VIC pixel clock PA14: GPIO group A bit 14	I I0
40	CIM_EXPOSURE	CIM_EXPOSURE: CIM exposure signal to sensor to generate snapshot PA15: GPIO group A bit 15	0 I0
41	CIM_VIC_HSYNC/I2S2_RX_DATA2	CIM_VIC_HSYNC: CIM/VIC fram sync I2S2_RX_DATA2: I2S2 data input bit 2 PA12: GPIO group A bit 12	I I I0
42	VIC_D8	VIC_D8: VIC DATA8 UART7_RXD: UART7 receiving data PA08: GPIO group A bit 8	I I I0
43	CIM_VIC_D7/I2S2_RX_MCLK	CIM_VIC_D7: CIM/VIC DATA7 UART6_TXD: UART6 transmitting data I2S2_RX_MCLK: I2S2 master clock output for input data PA07: GPIO group A bit 7	I 0 0 I0
44	CIM_VIC_D6/I2S3_TX_DATA3	CIM_VIC_D6: CIM/VIC DATA6 UART6_RXD: UART6 receiving data I2S3_TX_DATA3: I2S3 data output bit 3 PA06: GPIO group A bit 6	I I 0 I0

45	CIM_VIC_D0/I2S3_TX_MCLK	CIM_VIC_D0: CIM/VIC DATA0 UART4_CTS_N: UART4 Clear to send control I2S3_TX_MCLK: I2S3 master clock output for output data PA00: GPIO group A bit 0	I I 0 IO
46	VIC_D9/I2S2_RX_LRCK	VIC_D9: VIC DATA9 UART7_TXD: UART7 transmitting data I2S2_RX_LRCK: I2S2 LR clock input PA09: GPIO group A bit 9	I 0 I IO
47	CIM_VIC_D4/I2S3_TX_DATA1	CIM_VIC_D4: CIM/VIC DATA4 UART5_RXD: UART5 receiving data I2S3_TX_DATA1: I2S3 data output bit 1 PA04: GPIO group A bit 4	I I 0 IO
48	CIM_VIC_D2/I2S3_TX_LRCK	CIM_VIC_D2: CIM/VIC DATA2 UART4_RXD: UART4 receiving data I2S3_TX_LRCK: I2S3 LR clock output PA02: GPIO group A bit 2	I I 0 IO
49	CIM_VIC_D3/I2S3_TX_DATA0	CIM_VIC_D3: CIM/VIC DATA3 UART4_TXD: UART4 transmitting data I2S3_TX_DATA0: I2S3 data output bit 0 PA03: GPIO group A bit 3	I 0 0 IO
50	CIM_VIC_D1	CIM_VIC_D1: CIM/VIC DATA1 UART4_RTS_N: UART4 Request to send control PA01: GPIO group A bit 1	I 0 IO
51	CIM_VIC_D5/I2S3_TX_DATA2	CIM_VIC_D5: CIM/VIC DATA5 UART5_TXD: UART5 transmitting data I2S3_TX_DATA2: I2S3 data output bit 2 PA05: GPIO group A bit 5	I 0 0 IO
52	GND	GND	P
53	AUX4	AUX4	AI
54	AUX2	AUX2	AI
55	AUX0	AUX0	AI
56	AUX5	AUX5	AI
57	AUX1	AUX1	AI
58	AUX3	AUX3	AI
59	GND	GND	P
60	VDDIO_SD	VDDIO_SD	PO
61	GND	GND	P
62	VBATRTC	VBATRTC	PI
63	GND	GND	P

64	OTG_DP	OTG_DP	AIO
65	OTG_DM	OTG_DM	AIO
66	GND	GND	P
67	VBUS	VBUS	PI
68	USB_DETECT	USB_DETECT	I
69	USB_ID	USB_ID	I
70	MICLP	CODEC_MICLP	AI
71	MICLN	CODEC_MICLN	AI
72	MICBIAS	CODEC_MICBIAS	PO
73	HPOUTN	CODEC_HPOUTN	AO
74	HPOUTP	CODEC_HPOUTP	AO
75	GND	GND	P
76	MSC1_D3	MSC1_D3: MSC1 data bit 3 PWM7: PWM7 data output TCU3_IN1: TCU3 data input1 PE05: GPIO group E bit 5	IO O I IO
77	MSC1_D2	MSC1_D2: MSC1 data bit 2 PWM6: PWM6 data output TCU3_IN0: TCU3 data input0 PE04: GPIO group E bit 4	IO O I IO
78	MSC1_D1	MSC1_D1: MSC1 data bit 1 PWM5: PWM5 data output TCU2_IN1: TCU2 data input1 PE03: GPIO group E bit 3	IO O I IO
79	MSC1_D0	MSC1_D0: MSC1 data bit 0 PWM4: PWM4 data output TCU2_IN0: TCU2 data input0 PE02: GPIO group E bit 2	IO O I IO
80	MSC1_CMD	MSC1_CMD: MSC1 comand control PWM3: PWM3 data output TCU1_IN1: TCU1 data input1 PE01: GPIO group E bit 1	O O I IO
81	MSC1_CLK	MSC1_CLK: MSC1 clock output PWM2: PWM3 data output TCU1_IN0: TCU1 data input0 PE00: GPIO group E bit 0	O O I IO
82	GND	GND	P

83	RGMACO_TX_CLK/SPDIF_OUT	PWM14: PWM14 data output TCU7_IN0: TCU7 data input0 RGMACO_TX_CLK: RGMII0 TX clock SPDIF_OUT: Audio SPDIF format output I2C0_SDA: I2C0 serial data PC14: GPIO group C bit 14	0 I 0 0 IO IO
84	RGMACO_TXD2/I2S1_RX_DATA	PWM4: PWM4 data output TCU2_IN0: TCU2 data input0 RGMACO_TXD2: RGMII0 TX data bit 2 I2S1_RX_DATA: I2S1 data input SCC_SDA: Smart Card data PC04: GPIO group C bit 4	0 I 0 I IO IO
85	RGMACO_TX_EN/SSI1_DR	PWM10: PWM10 data output TCU5_IN0: TCU5 data input0 RGMACO_TX_EN: RGMII0 transmit enable SSI1_DR: SSI1 data input UART4_RTS_N: UART4 Request to send control PC10: GPIO group C bit 10	0 I 0 I 0 IO
86	RGMACO_TXD0/I2S1_RX_BCLK	PWM2: PWM2 data output TCU1_IN0: TCU1 data input0 RGMACO_TXD0: RGMII0 TX data bit 0 I2S1_RX_BCLK: I2S1 bit clock input UART7_TXD: UART7 transmitting data PC02: GPIO group C bit 2	0 I 0 I 0 IO
87	RGMACO_TXD1/I2S1_RX_LRCK	PWM3: PWM3 data output TCU1_IN1: TCU1 data input1 RGMACO_TXD1: RGMII0 TX data bit 1 I2S1_RX_LRCK: I2S1 LR clock input SCC_SCK: Smart Card clock PC03: GPIO group C bit 3	0 I 0 I 0 IO
88	RGMACO_TXD3/I2S1_TX_BCLK	PWM5: PWM5 data output TCU2_IN1: TCU2 data input1 RGMACO_TXD3: RGMII0 TX data bit 3 I2S1_TX_BCLK: I2S1 bit clock output UART5_RXD: UART5 receiving data PC05: GPIO group C bit 5	0 I 0 0 I IO
89	RGMACO_RXD1/I2S1_TX_DATA	PWM7: PWM7 data output TCU3_IN1: TCU3 data input1 RGMACO_RXD1: RGMII0 RX data bit 1 I2S1_TX_DATA: I2S1 data output UART6_RXD: UART6 receiving data PC07: GPIO group C bit 7	0 I I 0 I IO

90	RGMAC0_RX_DV/SSI1_DT	PWM11: PWM11 data output TCU5_IN1: TCU5 data input1 RGMAC0_RX_DV: RGMII0 RX data valid SSI1_DT: SSI1 data output UART4_RXD: UART4 receiving data PC11: GPIO group C bit 11	0 I I 0 I IO
91	RGMAC0_RXD0/I2S1_TX_LRCK	PWM6: PWM6 data output TCU3_IN0: TCU3 data input0 RGMAC0_RXD0: RGMII0 RX data bit 0 I2S1_TX_LRCK: I2S1 LR clock output UART5_TXD: UART5 transmitting data PC06: GPIO group C bit 6	0 I I 0 0 IO
92	RGMAC0_RXD3	PWM9: PWM9 data output TCU4_IN1: TCU4 data input1 RGMAC0_RXD3: RGMII0 RX data bit 3 SSI1_CE0_N: SSI1 chip select UART4_CTS_N: UART4 Clear to send control PC09: GPIO group C bit 9	0 I I 0 I IO
93	RGMAC0_RXD2/I2S1_TX_MCLK	PWM8: PWM8 data output TCU4_IN0: TCU4 data input0 RGMAC0_RXD2: RGMII0 RX data bit 2 I2S1_TX_MCLK: I2S1 master clock output for output data UART6_TXD: UART6 transmitting data PC08: GPIO group C bit 8	0 I I 0 0 IO
94	RGMAC0_RX_CLK/CIM_VIC_MCLK	PWM15: PWM15 data output TCU7_IN1: TCU7 data input1 RGMAC0_RX_CLK: RGMII0 RX clock input CIM_VIC_MCLK: CAMERA master clock output PC15: GPIO group C bit 15	0 I I 0 IO
95	RGMAC0_PHY_CLK/I2S1_RX_MCLK	PWM1: PWM1 data output RGMAC0_PHY_CLK: 50MHz clock output I2S1_RX_MCLK: I2S1 master clock output for input data UART7_RXD: UART7 receiving data PC01: GPIO group C bit 1	0 0 0 I I IO
96	RGMAC0_MDIO/SPDIF_IN	PWM13: PWM13 data output TCU6_IN1: TCU6 data input1 RGMAC0_MDIO: RGMII0 management data SPDIF_IN: Audio SPDIF format input I2C0_SCK: I2C0 serial clock PC13: GPIO group C bit 13	0 I IO I 0 IO

97	RGMACO_MDC/SSI1_CLK	PWM12: PWM12 data output TCU6_IN0: TCU6 data input0 RGMACO_MDC: RGMII0 management clock SSI1_CLK: SSI1 clock output UART4_TXD: UART4 transmitting data PC12: GPIO group C bit 12	0 I 0 0 0 IO
98	DMIC_IN1	DMIC_IN1: Dmic data in for dmic 2/3 UART1_RTS_N: UART1 Request to send control PC22: GPIO group C bit 22	I 0 IO
99	DMIC_CLK	DMIC_CLK: Digital MIC clock output PC20: GPIO group C bit 20	0 IO
100	DMIC_IN0	DMIC_IN0: Dmic data in for dmic 0/1 UART1_CTS_N: UART1 Clear to send control PC21: GPIO group C bit 21	I I IO
101	DMIC_IN2	DMIC_IN2: Dmic data in for dmic 4/5 UART1_RXD: UART1 receiving data I2C1_SCK: I2C1 serial clock NEMC_CS1_N: NEMC chip select1 PC23: GPIO group C bit 23	I I 0 0 IO
102	DMIC_IN3	DMIC_IN3: Dmic data in for dmic 6/7 UART1_TXD: UART1 transmitting data I2C1_SDA: I2C1 serial data NEMC_CS2_N: NEMC chip select2 PC24: GPIO group C bit 24	I 0 0 0 IO
103	GND	GND	P
104	RX_CLKN1	RX_CLKN1	AO
105	RX_CLKP1	RX_CLKP1	AO
106	RX_DATAP3	RX_DATAP3	AI
107	RX_DATAN3	RX_DATAN3	AI
108	RX_DATAN2	RX_DATAN2	AI
109	RX_DATAP2	RX_DATAP2	AI
110	RX_CLKN0	RX_CLKN0	AO
111	RX_CLKP0	RX_CLKP0	AO
112	RX_DATAP1	RX_DATAP1	AI
113	RX_DATAN1	RX_DATAN1	AI
114	RX_DATAPO	RX_DATAPO	AI
115	RX_DATANO	RX_DATANO	AI
116	DSI_DN0	TX_DATANO	AO
117	DSI_DPO	TX_DATAPO	AO

118	DSI_CLKP	TX_CLKP	A0
119	DSI_CLKN	TX_CLKN	A0
120	DSI_DP1	TX_DATAP1	A0
121	DSI_DN1	TX_DATAN1	A0
122	GND	GND	P
123	LCD_D4/SLCD_D4	SA4: NEMC Address4 LCD_D4: LCD DATA4 SLCD_D4: Smart LCD DATA4 PB04: GPIO group B bit 4	0 0 0 IO
124	LCD_D2/SLCD_D2	SA2: NEMC Address2 LCD_D2: LCD DATA2 SLCD_D2: Smart LCD DATA2 PB02: GPIO group B bit 2	0 0 0 IO
125	LCD_D3/SLCD_D3	SA3: NEMC Address3 LCD_D3: LCD DATA3 SLCD_D3: Smart LCD DATA3 PB03: GPIO group B bit 3	0 0 0 IO
126	LCD_D0/SLCD_D0	SA0: NEMC Address0 LCD_D0: LCD DATA0 SLCD_D0: Smart LCD DATA0 PB00: GPIO group B bit 0	0 0 0 IO
127	LCD_D7/SLCD_D7	SA7: NEMC Address7 LCD_D7: LCD DATA7 SLCD_D7: Smart LCD DATA7 PB07: GPIO group B bit 7	0 0 0 IO
128	LCD_D1/SLCD_D1	SA1: NEMC Address1 LCD_D1: LCD DATA1 SLCD_D1: Smart LCD DATA1 PB01: GPIO group B bit 1	0 0 0 IO
129	LCD_D5/SLCD_D5	SA5: NEMC Address5 LCD_D5: LCD DATA5 SLCD_D5: Smart LCD DATA5 PB05: GPIO group B bit 5	0 0 0 IO
130	LCD_D6/SLCD_D6	SA6: NEMC Address6 LCD_D6: LCD DATA6 SLCD_D6: Smart LCD DATA6 PB06: GPIO group B bit 6	0 0 0 IO
131	LCD_D21/RGMAC1_TX_CLK	SD5: NEMC DATA5 LCD_D21: LCD DATA21 RGMAC1_TX_CLK: RGMII1 TX clock PB21: GPIO group B bit 21	IO 0 0 IO



132	LCD_D8/SLCD_D8/RGMAC1_TXD0	SA8: NEMC Address8 LCD_D8: LCD DATA8 SLCD_D8: Smart LCD DATA8 RGMAC1_TXD0: RGMII1 TX data bit 0 PB08: GPIO group B bit 8	0 0 0 0 IO
133	LCD_D10/SLCD_D10/RGMAC1_TXD2	SA10: NEMC Address10 LCD_D10: LCD DATA10 SLCD_D10: Smart LCD DATA10 RGMAC1_TXD2: RGMII1 TX data bit 3 PB10: GPIO group B bit 10	0 0 0 0 IO
134	LCD_D9/SLCD_D9/RGMAC1_TXD1	SA9: NEMC Address9 LCD_D9: LCD DATA9 SLCD_D9: Smart LCD DATA9 RGMAC1_TXD1: RGMII1 TX data bit 1 PB09: GPIO group B bit 9	0 0 0 0 IO
135	LCD_D11/SLCD_D11/RGMAC1_TXD3	SA11: NEMC Address11 LCD_D11: LCD DATA11 SLCD_D11: Smart LCD DATA11 RGMAC1_TXD3: RGMII1 TX data bit 3 PB11: GPIO group B bit 11	0 0 0 0 IO
136	LCD_D17/RGMAC1_TX_EN	SD1: NEMC DATA1 LCD_D17: LCD DATA17 RGMAC1_TX_EN: RGMII1 transmit enable PB17: GPIO group B bit 17	10 0 0 IO
137	LCD_D22/RGMAC1_RX_CLK	SD6: NEMC DATA6 LCD_D22: LCD DATA22 I2C2_SCK: I2C2 serial clock RGMAC1_RX_CLK: RGMII0 RX clock PB22: GPIO group B bit 22	10 0 0 I IO
138	LCD_D13/SLCD_D13/RGMAC1_RXD1	RD_N: NEMC read enable LCD_D13: LCD DATA13 SLCD_D13: Smart LCD DATA RGMAC1_RXD1: RGMII1 RX data bit 1 PB13: GPIO group B bit 13	0 0 0 I IO
139	LCD_D14/SLCD_D14/RGMAC1_RXD2	WE_N: NEMC write enable LCD_D14: LCD DATA14 SLCD_D14: Smart LCD DATA14 RGMAC1_RXD2: RGMII1 RX data bit 2 PB14: GPIO group B bit 14	0 0 0 I IO

140	LCD_D12/SLCD_D12/RGMAC1_RXD0	SA12: NEMC Address12 LCD_D12: LCD DATA12 SLCD_D12: Smart LCD DATA12 RGMAC1_RXD0: RGMII1 RX data bit 0 PB12: GPIO group B bit 12	0 0 0 I IO
141	LCD_D15/SLCD_D15/RGMAC1_RXD3	WAIT_N: NEMC wait for external memory LCD_D15: LCD DATA15 SLCD_D15: Smart LCD DATA15 RGMAC1_RXD3: RGMII1 RX data bit 3 PB15: GPIO group B bit 15	I 0 0 I IO
142	LCD_D23/RGMAC1_PHY_CLK	SD7: NEMC DATA7 LCD_D23: LCD DATA23 I2C2_SDA: I2C2 serial data RGMAC1_PHY_CLK: 50MHz clock output PB23: GPIO group B bit 23	IO 0 IO 0 IO
143	LCD_D18/RGMAC1_RX_DV	SD2: NEMC DATA2 LCD_D18: LCD DATA18 RGMAC1_RX_DV: RGMII1 RX data valid PB18: GPIO group B bit 18	IO 0 I IO
144	LCD_D16	SD0: NEMC DATA0 LCD_D16: LCD DATA16 PB16: GPIO group B bit 16	IO 0 IO

## 2.2 引脚定义

注释:

1. I INPUT pin
2. O OUTPUT pin
3. IO INPUT&OUTPUT pin
4. AI Analog INPUT pin
5. AO Analog OUTPUT pin
6. AIO Analog INPUT & Analog OUTPUT pin
7. PI POWER input pin
8. PO POWER output pin



## 3 电气参数

### 3.1 最大范围

Table 3-1

	Min	Max	Unit
Operation Temperature	-40	85	°C
Storage Temperature	-65	150	°C
VSYS	-0.5	5.5	V

### 3.2 工作条件

Table 3-2

	Descriptions	Min	Typical	Max	Unit
T <sub>op</sub>	Operation Temperature	-40	25	85	°C
VIH18	Input high voltage for 1.8V I/O application	1.17	1.8	1.98	V
VIH18	Input low voltage for 1.8V I/O application	-0.3	0	0.63	V
VIH33	Input high voltage for 3.3V I/O application	2.0	3.3	3.465	V
VIH33	Input high voltage for 3.3V I/O application	-0.3	0	0.8	V

### 3.3 GPIO 管脚直流特性

Table 3-3 DC characteristics for VDDIO/VDDIORTC supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V <sub>T</sub>	Threshold point	0.82	0.89	0.97	V
V <sub>T+</sub>	Schmitt trig low to high threshold point	0.96	1.03	1.1	V
V <sub>T-</sub>	Schmitt trig high to low threshold point	0.64	0.75	0.86	V
V <sub>TPU</sub>	Threshold point with pull-up resistor enabled	0.81	0.88	0.97	V
V <sub>TPD</sub>	Threshold point with pull-down resistor enabled	0.82	0.89	0.98	V
V <sub>TPU+</sub>	Schmitt trig low to high threshold point with pull-up resistor enabled	0.95	1.02	1.09	V
V <sub>TPU-</sub>	Schmitt trig high to low threshold point with pull-down resistor enabled	0.63	0.75	0.85	V
V <sub>TPD+</sub>	Schmitt trig low to high threshold point with pull-down resistor enabled	0.96	1.05	1.11	V
V <sub>TPD-</sub>	Schmitt trig high to low threshold point with pull-up	0.65	0.76	0.86	V

	resistor enabled				
I <sub>L</sub>	Input Leakage Current @ V <sub>I</sub> =1.8V or 0V			±10	μA
I <sub>OZ</sub>	Tri-State output leakage current @ V <sub>I</sub> =1.8V or 0V			±10	μA
R <sub>PU</sub>	Pull-up Resistor	60	89	137	kΩ
R <sub>PD</sub>	Pull-down Resistor	61	104	196	kΩ
V <sub>OL</sub>	Output low voltage			0.45	V
V <sub>OH</sub>	Output high voltage	1.35			V
I <sub>OL</sub>	Low level output current @ V <sub>OL</sub> (max)	11.1	18.2	25.6	mA
I <sub>OH</sub>	High level output current @ V <sub>OH</sub> (min)	13.1	19.1	26.2	mA

**Table 3-4 DC characteristics for VDDIO33\_SD supplied pins for 1.8V application**

Symbol	Parameter	Min	Typical	Max	Unit	
V <sub>T</sub>	Threshold point	0.76	0.94	1.24	V	
V <sub>T+</sub>	Schmitt trig low to high threshold point	0.94	1.09	1.36	V	
V <sub>T-</sub>	Schmitt trig high to low threshold point	0.68	0.89	1.2	V	
V <sub>TPU</sub>	Threshold point with pull-up resistor enabled	0.74	0.92	1.22	V	
V <sub>TPD</sub>	Threshold point with pull-down resistor enabled	0.76	0.95	1.25	V	
V <sub>TPU+</sub>	Schmitt trig low to high threshold point with pull-up resistor enabled	0.93	1.07	1.34	V	
V <sub>TPU-</sub>	Schmitt trig high to low threshold point with pull-down resistor enabled	0.66	0.88	1.18	V	
V <sub>TPD+</sub>	Schmitt trig low to high threshold point with pull-down resistor enabled	0.95	1.1	1.388	V	
V <sub>TPD-</sub>	Schmitt trig high to low threshold point with pull-up resistor enabled	0.68	0.9	1.22	V	
I <sub>L</sub>	Input Leakage Current @ V <sub>I</sub> =1.8V or 0V			±10	μA	
I <sub>OZ</sub>	Tri-State output leakage current @ V <sub>I</sub> =1.8V or 0V			±10	μA	
R <sub>PU</sub>	Pull-up Resistor	33	59	91	kΩ	
R <sub>PD</sub>	Pull-down Resistor	34	61	108	kΩ	
V <sub>OL</sub>	Output low voltage			0.4	V	
V <sub>OH</sub>	Output high voltage	2.475			V	
I <sub>OL</sub>	Low level output current @ V <sub>OL</sub> (max)	(DS2,DS1,DS0) = 000	4.5	7.7	11.3	mA
		(DS2,DS1,DS0) = 001	6.7	11.4	16.7	mA
		(DS2,DS1,DS0) = 010	9	15.2	22.1	mA
		(DS2,DS1,DS0) = 011	11.2	18.8	27.3	mA
		(DS2,DS1,DS0) = 100	13.4	22.6	32.7	mA
		(DS2,DS1,DS0) = 101	15.6	26.2	37.8	mA
		(DS2,DS1,DS0) = 110	17.7	29.7	42.8	mA

		(DS2,DS1,DS0) = 111	19.9	33.2	47.7	mA
I <sub>OH</sub>	High level output current @ V <sub>OH</sub> (min)	(DS2,DS1,DS0) = 000	2.6	6.3	11.9	mA
		(DS2,DS1,DS0) = 001	3.8	9.4	17.7	mA
		(DS2,DS1,DS0) = 010	5.1	12.6	23.7	mA
		(DS2,DS1,DS0) = 011	6.4	15.7	29.4	mA
		(DS2,DS1,DS0) = 100	7.6	18.8	35.2	mA
		(DS2,DS1,DS0) = 101	8.9	21.8	40.9	mA
		(DS2,DS1,DS0) = 110	10.1	24.9	46.6	mA
		(DS2,DS1,DS0) = 111	11.4	27.9	52.2	mA

**Table 3-5 DC characteristics for VDDIO33\_SD supplied pins for 3.3V application**

Symbol	Parameter	Min	Typical	Max	Unit	
V <sub>T</sub>	Threshold point	1.39	1.5	1.65	V	
V <sub>T+</sub>	Schmitt trig low to high threshold point	1.62	1.75	1.9	V	
V <sub>T-</sub>	Schmitt trig high to low threshold point	1.18	1.29	1.44	V	
V <sub>TPU</sub>	Threshold point with pull-up resistor enabled	1.36	1.48	1.64	V	
V <sub>TPD</sub>	Threshold point with pull-down resistor enabled	1.4	1.52	1.66	V	
V <sub>TPU+</sub>	Schmitt trig low to high threshold point with pull-up resistor enabled	1.62	1.75	1.89	V	
V <sub>TPU-</sub>	Schmitt trig high to low threshold point with pull-down resistor enabled	1.16	1.28	1.43	V	
V <sub>TPD+</sub>	Schmitt trig low to high threshold point with pull-down resistor enabled	1.64	1.77	1.91	V	
V <sub>TPD-</sub>	Schmitt trig high to low threshold point with pull-up resistor enabled	1.19	1.31	1.45	V	
I <sub>L</sub>	Input Leakage Current @ VI=1.8V or 0V			±10	μA	
I <sub>OZ</sub>	Tri-State output leakage current @ VI=1.8V or 0V			±10	μA	
R <sub>PU</sub>	Pull-up Resistor	34	51	81	kΩ	
R <sub>PD</sub>	Pull-down Resistor	35	51	88	kΩ	
V <sub>OL</sub>	Output low voltage			0.4	V	
V <sub>OH</sub>	Output high voltage	2.4			V	
I <sub>OL</sub>	Low level output current @ V <sub>OL</sub> (max)	(DS2,DS1,DS0) = 000	2.8	5.4	9.8	mA
		(DS2,DS1,DS0) = 001	4.1	8.0	14.6	mA
		(DS2,DS1,DS0) = 010	5.5	10.7	19.4	mA
		(DS2,DS1,DS0) = 011	6.8	13.2	23.9	mA
		(DS2,DS1,DS0) = 100	8.2	15.9	28.7	mA
		(DS2,DS1,DS0) = 101	9.6	18.4	33.2	mA
		(DS2,DS1,DS0) = 110	10.9	20.9	37.6	mA

		(DS2,DS1,DS0) = 111	12.2	23.4	42.0	mA
I <sub>OH</sub>	High level output current @ V <sub>OH</sub> (min)	(DS2,DS1,DS0) = 000	4.4	7.6	13.5	mA
		(DS2,DS1,DS0) = 001	6.6	11.4	20.2	mA
		(DS2,DS1,DS0) = 010	8.8	15.2	26.9	mA
		(DS2,DS1,DS0) = 011	10.9	18.9	33.5	mA
		(DS2,DS1,DS0) = 100	13.1	22.6	40.1	mA
		(DS2,DS1,DS0) = 101	15.2	26.3	46.7	mA
		(DS2,DS1,DS0) = 110	17.4	30.1	53.3	mA
		(DS2,DS1,DS0) = 111	19.6	23.7	59.7	mA

**Table 3-6 DC characteristics for VDDIO33/VDDIO18 supplied pins for 3.3V application**

Symbol	Parameter	Min	Typical	Max	Unit	
V <sub>T</sub>	Threshold point	1.02	1.17	1.36	V	
V <sub>T+</sub>	Schmitt trig low to high threshold point	1.22	1.34	1.5	V	
V <sub>T-</sub>	Schmitt trig high to low threshold point	0.96	1.13	1.33	V	
V <sub>TPU</sub>	Threshold point with pull-up resistor enabled	1	1.15	1.34	V	
V <sub>TPD</sub>	Threshold point with pull-down resistor enabled	1.03	1.19	1.38	V	
V <sub>TPU+</sub>	Schmitt trig low to high threshold point with pull-up resistor enabled	1.21	1.32	1.47	V	
V <sub>TPU-</sub>	Schmitt trig high to low threshold point with pull-down resistor enabled	0.94	1.1	1.3	V	
V <sub>TPD+</sub>	Schmitt trig low to high threshold point with pull-down resistor enabled	1.23	1.35	1.52	V	
V <sub>TPD-</sub>	Schmitt trig high to low threshold point with pull-up resistor enabled	0.97	1.14	1.34	V	
I <sub>L</sub>	Input Leakage Current @ V <sub>I</sub> =1.8V or 0V			±10	μA	
I <sub>OZ</sub>	Tri-State output leakage current @ V <sub>I</sub> =1.8V or 0V			±10	μA	
R <sub>PU</sub>	Pull-up Resistor	26	46	71	kΩ	
R <sub>PD</sub>	Pull-down Resistor	27	48	103	kΩ	
V <sub>OL</sub>	Output low voltage			0.4	V	
V <sub>OH</sub>	Output high voltage	2.4			V	
I <sub>OL</sub>	Low level output current @ V <sub>OL</sub> (max)	(DS2,DS1,DS0) = 000	4	6.3	8.9	mA
		(DS2,DS1,DS0) = 001	6	9.4	13.3	mA
		(DS2,DS1,DS0) = 010	8	12.5	17.6	mA
		(DS2,DS1,DS0) = 011	9.9	15.5	21.8	mA
		(DS2,DS1,DS0) = 100	11.9	18.6	26.1	mA
		(DS2,DS1,DS0) = 101	13.9	21.6	30.2	mA
		(DS2,DS1,DS0) = 110	15.8	24.5	34.2	mA



		(DS2,DS1,DS0) = 111	17.7	27.4	38.1	mA
I <sub>OH</sub>	High level output current @ V <sub>OH</sub> (min)	(DS2,DS1,DS0) = 000	5.9	9.3	14.2	mA
		(DS2,DS1,DS0) = 001	8.8	13.9	21.2	mA
		(DS2,DS1,DS0) = 010	11.7	18.5	28.2	mA
		(DS2,DS1,DS0) = 011	14.6	23.1	35.2	mA
		(DS2,DS1,DS0) = 100	17.5	27.7	42.2	mA
		(DS2,DS1,DS0) = 101	20.3	32.2	49.1	mA
		(DS2,DS1,DS0) = 110	23.2	36.8	56	mA
		(DS2,DS1,DS0) = 111	26.1	41.3	62.8	mA

**Table 3-7 DC characteristics for VDDIO33\_CIM/VDDIO18\_CIM supplied pins for 3.3V application**

Symbol	Parameter	Min	Typical	Max	Unit	
V <sub>T</sub>	Threshold point	0.76	0.94	1.24	V	
V <sub>T+</sub>	Schmitt trig low to high threshold point	0.94	1.09	1.37	V	
V <sub>T-</sub>	Schmitt trig high to low threshold point	0.68	0.89	1.21	V	
V <sub>TPU</sub>	Threshold point with pull-up resistor enabled	0.74	0.93	1.22	V	
V <sub>TPD</sub>	Threshold point with pull-down resistor enabled	0.76	0.95	1.26	V	
V <sub>TPU+</sub>	Schmitt trig low to high threshold point with pull-up resistor enabled	0.93	1.08	1.34	V	
V <sub>TPU-</sub>	Schmitt trig high to low threshold point with pull-down resistor enabled	0.67	0.88	1.18	V	
V <sub>TPD+</sub>	Schmitt trig low to high threshold point with pull-down resistor enabled	0.95	1.1	1.38	V	
V <sub>TPD-</sub>	Schmitt trig high to low threshold point with pull-up resistor enabled	0.68	0.9	1.22	V	
I <sub>L</sub>	Input Leakage Current @ V <sub>I</sub> =1.8V or 0V			±10	μA	
I <sub>OZ</sub>	Tri-State output leakage current @ V <sub>I</sub> =1.8V or 0V			±10	μA	
R <sub>PU</sub>	Pull-up Resistor	33	59	91	kΩ	
R <sub>PD</sub>	Pull-down Resistor	34	61	108	kΩ	
V <sub>OL</sub>	Output low voltage			0.4	V	
V <sub>OH</sub>	Output high voltage	2.4			V	
I <sub>OL</sub>	Low level output current @ V <sub>OL</sub> (max)	(DS1,DS0) = 00	2.8	5.4	9.8	mA
		(DS1,DS0) = 01	4.1	8.0	14.6	mA
		(DS1,DS0) = 10	5.5	10.6	19.3	mA
		(DS1,DS0) = 11	6.8	13.2	23.8	mA
I <sub>OH</sub>	High level output current @ V <sub>OH</sub> (min)	(DS1,DS0) = 00	4.4	7.6	13.5	mA
		(DS1,DS0) = 01	6.6	11.4	20.2	mA

	(DS1,DS0) = 10	8.8	15.2	26.9	mA
	(DS1,DS0) = 11	10.9	18.9	33.6	mA

**Table 3-8DC characteristics for VDDIO33\_CIM/VDDIO18\_CIM supplied pins for 1.8V application**

Symbol	Parameter	Min	Typical	Max	Unit	
V <sub>T</sub>	Threshold point	0.85	0.95	1.08	V	
V <sub>T+</sub>	Schmitt trig low to high threshold point	0.97	1.06	1.17	V	
V <sub>T-</sub>	Schmitt trig high to low threshold point	0.7	0.82	0.94	V	
V <sub>TPU</sub>	Threshold point with pull-up resistor enabled	0.85	0.95	1.07	V	
V <sub>TPD</sub>	Threshold point with pull-down resistor enabled	0.86	0.96	1.09	V	
V <sub>TPU+</sub>	Schmitt trig low to high threshold point with pull-up resistor enabled	0.97	1.06	1.16	V	
V <sub>TPU-</sub>	Schmitt trig high to low threshold point with pull-down resistor enabled	0.69	0.81	0.93	V	
V <sub>TPD+</sub>	Schmitt trig low to high threshold point with pull-down resistor enabled	0.98	1.07	1.18	V	
V <sub>TPD-</sub>	Schmitt trig high to low threshold point with pull-up resistor enabled	0.7	0.82	0.95	V	
I <sub>L</sub>	Input Leakage Current @ VI=1.8V or 0V			±10	μA	
I <sub>oZ</sub>	Tri-State output leakage current @ VI=1.8V or 0V			±10	μA	
R <sub>PU</sub>	Pull-up Resistor	33	59	90	kΩ	
R <sub>PD</sub>	Pull-down Resistor	34	61	95	kΩ	
V <sub>OL</sub>	Output low voltage			0.45	V	
V <sub>OH</sub>	Output high voltage	1.4			V	
I <sub>OL</sub>	Low level output current @ V <sub>OL</sub> (max)	(DS1,DS0) = 00	4.5	7.6	11.2	mA
		(DS1,DS0) = 01	6.7	11.4	16.6	mA
		(DS1,DS0) = 10	8.9	15.1	22	mA
		(DS1,DS0) = 11	11.1	18.7	27.2	mA
I <sub>OH</sub>	High level output current @ V <sub>OH</sub> (min)	(DS1,DS0) = 00	2.6	6.3	11.9	mA
		(DS1,DS0) = 01	3.8	9.5	17.8	mA
		(DS1,DS0) = 10	5.1	12.6	23.7	mA
		(DS1,DS0) = 11	6.4	15.7	29.4	mA

### 3.4 功耗

请参阅 rd\_X2000\_Halley5\_coreboard\_v1\_0 功率测试报告。

## 4 机械尺寸

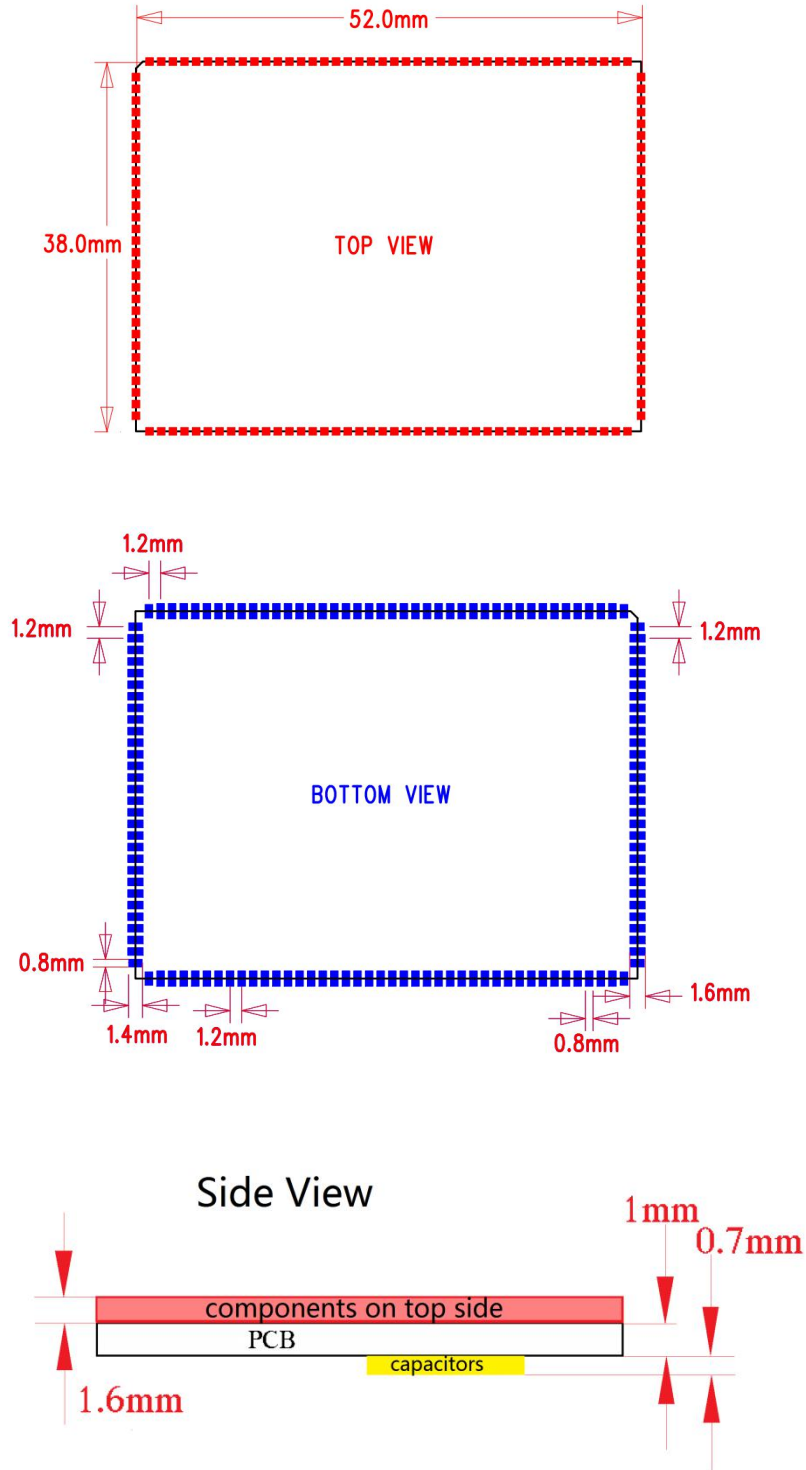


图 4-1 机械尺寸(单位, mm)

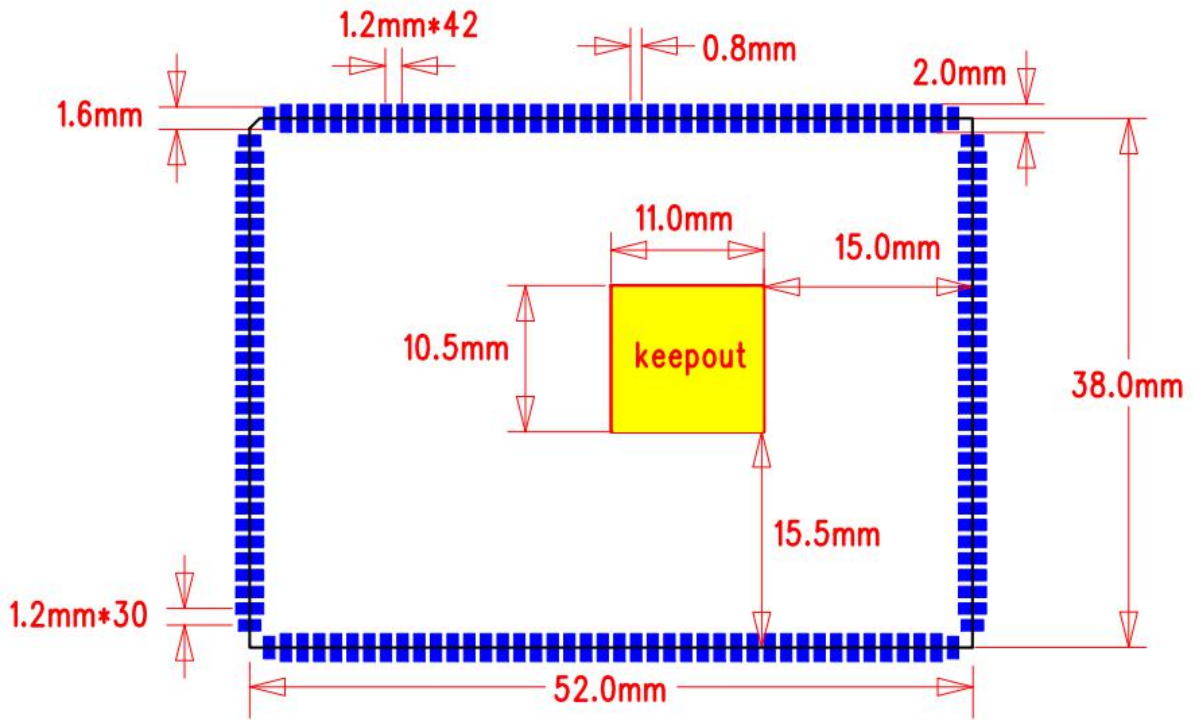


图 4-2 推荐的 PCB 封装焊盘尺寸(单位, mm)